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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,366	07/27/2001	Yasuhito Suzuki	50090-309	6983

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,366	SUZUKI ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4-6, 8 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,146,919 to Tandy.

Regarding claim 1, Tandy (figures 5-6) teaches a semiconductor package comprising:

a die pad (a portion of lead is formed under chip [102]);

a die (102) mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad;

a plurality of outer leads (118) electrically connected to electrodes of the die (102) by bonding wires (110), respectively; and

a sealing member (120) sealing the die (102), the bonding wires (110), parts of the outer leads (118) and a part of the die pad (a portion of lead is formed under chip [102]), and having an uppermost surface over the upper surface of the die (102) and a lower surface under the lower surface of the die (102);

wherein the outer leads (118) extend at least from a plane including the lower surface of the sealing member (a lower portion of the encapsulant [120]) to beyond that of the uppermost surface of the sealing member (an upper portion of the encapsulant [120]), each of the outer leads (118) comprising an upper electrical connecting surface located above the uppermost surface of the sealing member (an upper portion of the encapsulant [120]), and a lower electrical connecting surface located at the lower surface of the sealing member (a lower portion of the encapsulant [120]).

Regarding claim 2, Tandy teaches the upper electrical connecting surfaces of the outer leads (118) lie outside an area over the uppermost surface of the sealing member (an upper portion of the encapsulant [120]).

Regarding claim 4, Tandy teaches the outer leads (a portion of the outer lead [118]) are formed in an L-shape.

Regarding claim 5, Tandy (figures 5-6) teaches a semiconductor package comprising:

a plurality of semiconductor packages arranged to be stacked up on a printed wiring board (the bottom lead surface [114] of the outer lead [118], which is formed on the circuit board [printed wiring board]) (column 4, lines 28-32) with outer leads (118) included therein; wherein each of the plurality of semiconductor packages comprises,

a die pad (a portion of lead is formed under chip [102]);

a die (102) mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad (a portion of lead is formed under chip [102]);

the outer leads (118) electrically connected to electrodes of the die (102) by bonding wires (110), respectively; and

a sealing member (120) sealing the die (102), the bonding wires (110), parts of the outer leads (118) and a part of the die pad (a portion of lead is formed under chip [102]), and having an uppermost surface over the upper surface of the die (102) and a lower surface under the lower surface of the die (102);

wherein the outer leads (118) extend at least from a plane including the lower surface of the sealing member (a lower portion of the encapsulant [120]) to beyond that of the uppermost surface of the sealing member (an upper portion of the encapsulant [120]), each of the outer leads (118) comprising an upper electrical connecting surface located above the uppermost surface of the sealing member (an upper portion of the encapsulant [120]), and a lower electrical connecting surface located at the lower surface of the sealing member (a lower portion of the encapsulant [120]).

Regarding claim 6, Tandy teaches the upper electrical connecting surfaces of the outer leads (118) lie outside an area over the uppermost surface of the sealing member (an upper portion of the encapsulant [120]).

Regarding claim 8, Tandy teaches the outer leads (a portion of the outer lead [118]) are formed in an L-shape.

Regarding claim 15, Tandy (figures 5-6) teaches a semiconductor package comprising:

a plurality of semiconductor packages arranged to be mounted on a printed wiring board (the bottom lead surface [114] of the outer leads [118], which is formed on a circuit board [printed wiring board]) (column 4, lines 28-32), wherein each of the plurality of semiconductor packages comprises,

a die pad (a portion of lead is formed under chip [102]);

a die (102) mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad (a portion of lead is formed under chip [102]);

a plurality of outer leads (118) electrically connected to electrodes of the die (102) by bonding wires (110), respectively; and

a sealing member (120) sealing the die (102), the bonding wires (110), parts of the outer leads (118) and a part of the die pad (a portion of lead is formed under chip [102]), and having an uppermost surface over the upper surface of the die (102) and a lower surface under the lower surface of the die (102);

wherein the outer leads (118) extend at least from a plane including the lower surface of the sealing member (a lower portion of the encapsulant [120]) to beyond that of the uppermost surface of the sealing member (an upper portion of the encapsulant [120]), each of the outer leads (118) comprising an upper electrical connecting surface located above the uppermost surface of the sealing member (an upper portion of the encapsulant [120]), and a lower electrical connecting surface located at the lower surface of the sealing member (a lower portion of the encapsulant [120]).

Tandy teaches the bottom lead surface (114) of the outer lead (118), which is formed on a circuit board (printed wiring board) (column4, lines 28-32). Therefore, it inherently teaches each of the semiconductor packages is arranged to be mounted on the printed wiring board such that the uppermost surface of the sealing member faces the printed wiring board.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,146,919 to Tandy.

The disclosures of Tandy are discussed as applied to claims 1-2 and 4 above.

Regarding claims 3 and 7, Tandy differs from the claimed invention by not showing the sealing member has four sides surrounded by the outer leads. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the sealing member has four sides surrounded by the outer leads because they increase the number of external connections between the die and the external circuit.

5. Claims 9-12, 14, 16-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,146,919 to Tandy in view of US Patent No. 5,644,163 to Tsuji.

Regarding claim 9, Tandy (figures 5-6) teach a semiconductor package comprising:

a die pad (a portion of lead is formed under chip [102]);

a die (102) mounted on the die pad and having an upper surface and a lower surface, the lower surface facing the die pad;

the outer leads (118) electrically connected to electrodes of the die (102) by bonding wires (110), respectively; and

a sealing member (120) sealing therein the die (102), the bonding wires (110), parts of the outer leads (118) and a part of the die pad (a portion of lead is formed under chip [102]), and having an upper surface over the upper surface of the die (102) and a lower surface under the lower surface of the die (102);

wherein the outer leads (118) have a height from a plane including the lower surface of the sealing member (a lower portion of the encapsulant [120]) greater than that of the upper surface of the sealing member (an upper portion of the encapsulant [120]) from the same plane, each of the outer leads (118) comprising an upper electrical connecting surface located above the upper surface of the sealing member (an upper portion of the encapsulant [120]), and a lower electrical connecting surface located at the lower surface of the sealing member (a lower portion of the encapsulant [120]).

Tandy teaches the bottom lead surface (114) of the outer leads (118), which is formed on a circuit board (printed wiring board) (column 4, lines 28-32). Therefore, it inherently teaches a plurality of semiconductor packages arranged to be mounted on a printed wiring board, each semiconductor package having an upper surface of a sealing member thereof facing the printed wiring board.

Tandy differs from the claimed invention by not showing forming electrodes on the printed wiring board. However, Tsuji teaches providing electrodes on the circuit board (printed wiring board) (column 7, lines 1-5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsuji into the device taught by Tandy because it provides interconnect between the semiconductor device and the external device. The combined device shows outer leads thereof connected to

electrodes formed on the printed wiring board and wherein each of the plurality of semiconductor packages.

Regarding claim 10, the combined device shows the upper electrical connecting surfaces of the outer leads (Tandy; 118) lie outside an area over the uppermost surface of the sealing member (Tandy; an upper portion of the encapsulant [120]).

Regarding claim 11, Tandy and Tsuji differ from the claimed invention by not showing the sealing member has four sides surrounded by the outer leads. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the sealing member has four sides surrounded by the outer leads because they increase the number of external connections between the die and the external circuit.

Regarding claim 12, the combined device shows the outer leads (Tandy; a portion of the outer lead [118]) are formed in an L-shape.

Regarding claim 14, Tandy teaches the bottom lead surface (114) of the outer lead (118), which is formed on a circuit board (printed wiring board) (column4, lines 28-32). Therefore, it inherently teaches each of the semiconductor packages is arranged to be mounted on the printed wiring board such that the upper surface of the sealing member faces that of another semiconductor package through the printed wiring board.

Regarding claim 16, the combined device shows the upper electrical connecting surfaces of the outer leads (Tandy; 118) lie outside an area over the upper surface of the sealing member (Tandy; an upper portion of the encapsulant [120]).

Regarding claim 17, Tandy and Tsuji differ from the claimed invention by not showing the sealing member has four sides surrounded by the outer leads. It would have been obvious to

one having ordinary skill in the art at the time the invention was made for the sealing member has four sides surrounded by the outer leads because they increase the number of external connections between the die and the external circuit.

Regarding claim 18, the combined device shows the outer leads (Tandy; a portion of the outer lead [118]) are formed in an L-shape.

Regarding claim 20, Tandy teaches the bottom lead surface (114) of the outer lead (118), which is formed on a circuit board (printed wiring board) (column4, lines 28-32). Therefore, it inherently teaches each of the semiconductor packages is arranged to be mounted on the printed wiring board such that the uppermost surface of the sealing member faces that of another semiconductor package through the printed wiring board.

6. Claims 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tandy in view of Tsuji, and further in view of US Patent No. 5,585,671 to Nagesh et al.

Regarding claims 13 and 19, the disclosures of Tandy and Tsuji are discussed as applied to claims 9-12, 14, 16-18 and 20 above.

Tandy and Tsuji differ from the claimed invention by not showing the die pad of the semiconductor package is provided on its exposed surface with a cooling fin. However, Nagesh et al. (figures 1, 3, 3A) teach the heat sink (32), which is provided on the die pad (20) of the semiconductor chip (12). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nagesh et al. into the device taught by Tandy and Tsuji because it dissipates heat from the die.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
April 26, 2004

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